BAJOPMAS JOURNAL 16(1): 20 – 26
Printed in Bayero University, Kano - Nigeria.

EFFECT OF HOLE MOBILITY VARIATION ON SHORT CHANNEL EFFECTS IN NANOSCALE DOUBLE GATE FinFETs

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ABSTRACT
This work presents an investigation into the impact of hole mobility variations on short channel effects (SCEs) in different FinFETs using semiconductor fin materials. Using the PADRE simulator, we simulated FinFETs made of Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN), and Silicon (Si). The study involved analyzing performance metrics, including Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), and Threshold Voltage roll-off. The study showed that variations in hole mobility do not significantly impact short channel issues in FinFETs. However, there is a notable shift in short channel effects observed in GaAs-FinFETs with higher hole mobilities. Despite consistent short channel effects, GaAs-FinFETs demonstrated superior performance in terms of DIBL with lowest value of 8.28 mV/V at at hole mobilities of 1400 cm^2/Vs and 1500 cm^2/Vs, and threshold voltage with lowest value of 0.427 V at (100-1300) cm^2/Vs. On the other hand, GaN-FinFET outperformed other FinFETs in terms of subthreshold swing by exhibiting lowest value of 63.95 mV/dec at hole mobilities of 1400 cm^2/Vs and 1500 cm^2/Vs. The study concludes that while variations in hole mobility do not significantly affect short channel issues in FinFETs, there is a distinct change observed in short channel effects in GaAs-FinFETs at higher hole mobilities. Understanding the relationship between hole mobility variations and short channel effects enables designers to optimize device structures and material choices for better overall performance.

Keywords: DIBL, FinFETs, GaAs, GaSb, Hole Mobility, SCEs,

1.0 Introduction
The pursuit of miniaturization in transistors is at the forefront of nanoscale technology, catalyzing transformative developments in the field of semiconductors [1-7], by facilitating the integration of hundreds of circuits on a single chip through Very Large Scale and Ultra-Large Scale Integrations. However, this reduction in the size of the transistor leads to the occurrence of some impediments to the operation of the MOSFET. These restrictions are known as short channel effects [8-14]. To tackle these challenges, a special structure called fin Field Effect Transistor standout to be a prospective electronic device [15-30] due to its improved scalability and ability to control the SCEs. The operational capabilities of nanoscale FinFETs are advancing to the point that quantum mechanical phenomena, such as quantum confinement effects, are becoming apparent [31-32]. This confinement alters the energy band structure of the material, leading to discrete energy levels and affecting electron mobility. In order to achieve greater downsizing and performance enhancement, it becomes important to investigate the delicate interplay between device dimensions, material characteristics, SCEs, and hole mobility in FinFET devices. The exploration of hole mobility in FinFET devices and its effects on short-channel effects is essential for optimizing device performance, reducing power consumption, and enabling further scaling of semiconductor technologies.

The impact of Short-Channel Effects (SCEs) on the performance of FinFETs has been reported in literature [33-40]. However, to the best of our knowledge no study has been reported on the effect of hole mobility on short channel effects.

This work aims at thoroughly investigating the impact of electron mobility variations on short channel effects in nanoscale double gate FinFET devices using Si, GaSb, GaN and GaAs as channel materials. The study focused on significant performance metrics: DIBL, SS, and threshold voltage roll-off, crucial in the determination of device performance. Simulations will be conducted using the PADRE Simulator, known for semiconductor device modeling. This research seeks to provide insights into optimizing FinFET performance and advancing semiconductor technology towards greater efficiency and functionality in nanoscale electronic devices.

1.1 Device Structure

Figure 1 shows the device structure of an n-channel double gate FinFET. The structure includes key components such as the source, drain, gate length (channel length), and channel width (fin width or fin thickness). Before forming the gate contact, the oxide is applied to the fin's top surface, as well as both sides of the side walls. The side wall's oxide thicknesses are Tox1 and Tox2.

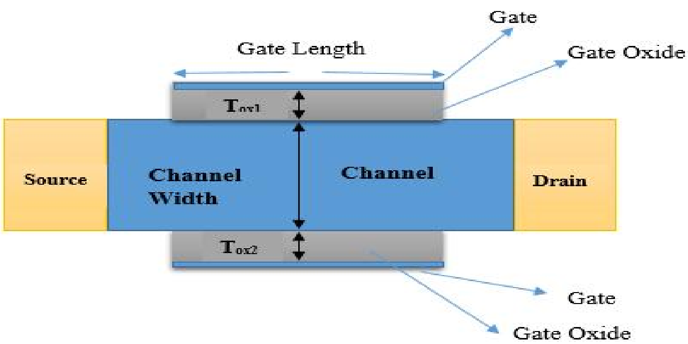

Figure 1. Two-Dimensional Double Gate FinFET

2. Materials and Method

This section describes the materials and the method that were used during the device simulation.

2.1 Materials

The materials used in this research are Si, GaAs, GaSb and GaN as fin (channel) materials, silicon dioxide (SiO_2) as the gate dielectric, Silicon as base substrate and MuGFET simulation tool.

2.2 Method

The device simulation was carried out using the PADRE simulator from the MuGFET tool. The effect of hole mobility on SCEs was examined in FinFETs using various semiconductor materials. The study focused on GaAs, GaSb, GaN, and Si FinFETs, analyzing significant performance metrics such as DIBL, SS, and threshold voltage roll-off. The oxide thickness employed was 2 nm, channel width was 10 nm, gate length was 45 nm, and hole mobility ranged from 100 to 1500 cm2/Vs. During the simulation, the drain/source doping was set at 1×10^{16} cm^{-3} and the channel doping concentration was maintained at 1×10^{19} cm^{-3}. While the gate bias was varied between 0 V and 1 V, and the drain bias was set between 0.05 V and 1 V. The parameters are listed in Table 1.

Table 1: Parameter Specifications used in this simulation

Parameter	Value
Gate Length	45 nm
Electron Mobility	(100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 150) cm^2/Vs
Channel Width	10 nm
Channel Doping Concentration	1×10^{16} cm^{-3}
Source/Drain Doping Concentration	1×10^{19} cm^{-3}
Drain Bias	0.05 V, 1.0 V
Gate Bias	0 V to 1.0 V

3. Results and Discussion

The effects of hole mobility on the three SCEs are presented here.

3.1 Impact of Hole Mobility Variations on DIBL

The impact of hole mobility variations on DIBL in DG-FinFET is presented in Figure 2 with diverse semiconductors as fin (channel) materials which include GaAs, GaSb, GaN and Si. Observations from the figure indicate that the four FinFETs maintained constant DIBL characteristics over the explored hole mobility range. This consistent trend indicates that DIBL is not significantly influenced by the variations in the hole mobility within the considered range. However, sudden fall in the DIBL value to 8.28 Mv/v at hole mobilities of 1400 cm^2/Vs and 1500 cm^2/Vs shoots GaAs-FinFET to outperform the other three FinFETs in terms of DIBL.This change may suggest that GaAs exhibits unique characteristics or responses to variations in hole mobility compared to the other materials (GaSb, GaN, and Si).

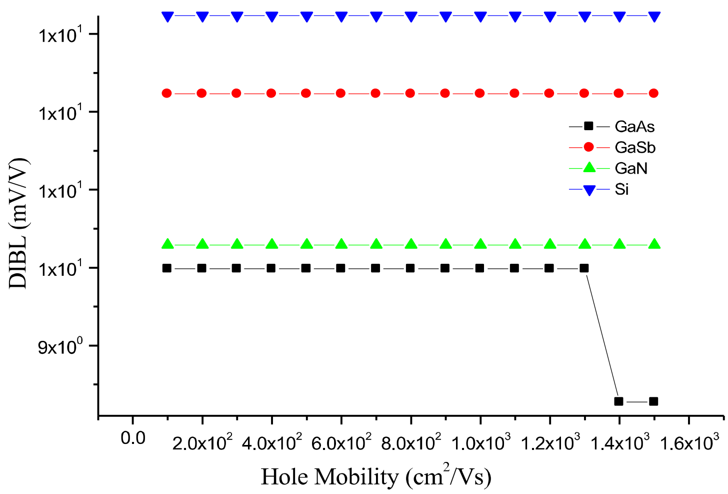

Figure 2. DIBL Vs Hole Mobility

3.2 Impact of Hole Mobility Variations on Subthreshold Swing

The impact of hole mobility variations on the subthreshold swing in nanoscale DG-FinFET employing GaAs, GaSb, GaN and Si as fin materials is presented in Figure 3. It can be observed from the figure that the four FinFETs maintained consistent subthreshold swing across the hole mobility range signifying that SS is not influenced by the variations of hole mobility for the range of values considered. However, there was a sudden fall in the SS observed in GaAs-FinFET at the hole mobilities of 1400 cm^2/Vs and 1500 cm^2/Vs. This change may suggest that GaAs exhibits unique characteristics or responses to variations in hole mobility compared to the other materials (GaSb, GaN, and Si). On the other hand, GaN-FinFET exhibits constant least DIBL value of 63.95 mV/dec across the considered hole mobility range signifying its superiority in terms of SS compared with the other three FinFETs.

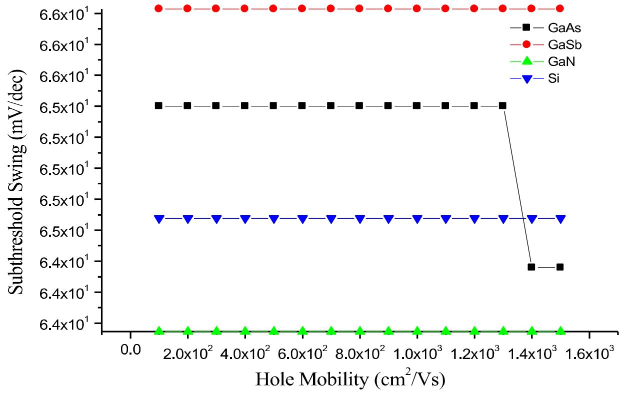

Figure 3. Subthreshold Swing Vs Hole Mobility

3.3 Impact of Hole Mobility Variations on Threshold Voltage

It can be observed from the figure that the four FinFETs maintained consistent subthreshold swing across the hole mobility range signifying that threshold voltage is not influenced by the variations of hole mobility for the range of values considered. However, there was a sudden rise in the threshold voltage observed in GaAs-FinFET at the hole mobilities of 1400 cm^2/Vs and 1500 cm^2/Vs. This change may suggest that GaAs exhibits unique characteristics or responses to variations in hole mobility compared to the other materials (GaSb, GaN, and Si). GaAs-FinFET exhibits lowest threshold voltage of 0.47 V at the electron mobilities of (100-1300) cm^2/Vs.

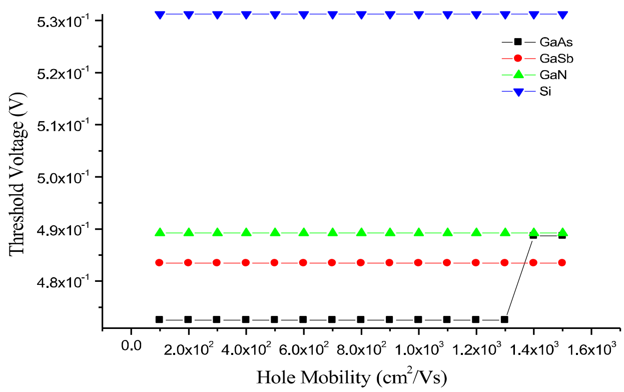

Figure 4. Threshold Voltage Vs Hole Mobility

4. Conclusion

We examined the complex relationship between hole mobility in fin materials and short channel effects in nanoscale double gate FinFETs, utilizing various semiconductor channel materials including GaAs, GaSb, GaN, and Si. The study indicated that variations in hole mobility do not significantly impact short channel issues in FinFETs. However, there was a notable shift in short channel effects observed in GaAs-FinFETs with higher hole mobilities. Despite consistent short channel effects, GaAs-FinFETs demonstrated superior performance in terms of DIBL and threshold voltage compared to other FinFETs. Conversely, GaN-FinFETs outperformed other FinFETs in terms of subthreshold swing. The study concludes that while variations in hole mobility do not significantly affect short channel issues in FinFETs overall, there is a distinct change observed in short channel effects in GaAs-FinFETs at higher hole mobilities. This finding contributes to the advancement of FinFET technology, which is essential for achieving miniaturization and performance enhancement in semiconductor devices. Further research could explore the underlying mechanisms causing the sudden change in short channel effects in GaAs-FinFETs at higher hole mobilities. Investigating the specific factors, such as material properties or device characteristics that contribute to this phenomenon would provide valuable insights.

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